II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, or versions, of claims.

1. (Currently Amended) A method of modeling for use with an integrated circuit (IC) design, the method comprising ~~the steps of~~:

partitioning an edge of a shape in the IC design into a plurality of intervals; and

assigning at least one dimension to each interval;

wherein the partitioning includes:

generating a core Voronoi diagram for the shape, the core Voronoi diagram being generated based on a $L\infty$ metric, the L_∞ metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points; and

partitioning the edge based on a core element for each vertex of the core Voronoi diagram, the core element being one of a largest possible core element and a smallest possible core element; and.

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

2. (Cancelled).

3. (Previously Presented) The method of claim 1, wherein the assigning is based on a Euclidean metric.

4-6. (Cancelled).

7. (Original) The method of claim 1, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

8. (Original) The method of claim 1, wherein the dimension is a function of another dimension.

9. (Currently Amended) The method of claim 1, further comprising ~~the step of~~ using the at least one dimension to evaluate a check rule.

10. (Original) The method of claim 9, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

11. (Original) The method of claim 1, wherein each concave vertex of the shape is an interval.

12. (Currently Amended) An integrated circuit (IC) modeling system comprising:

means for partitioning an edge of a shape in the IC design into a plurality of intervals; and

means for assigning at least one dimension to each interval;

wherein the partitioning means includes:

means for generating a core Voronoi diagram for the shape, the core Voronoi diagram being generated based on a $L\infty$ metric, the L_∞ metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points; and

means for partitioning the edge based on a core element for each vertex of the core Voronoi diagram, the core element being one of a largest possible core element and a smallest possible core element; and.

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible..

13. (Cancelled).

14-16. (Cancelled).

17. (Original) The system of claim 12, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

18. (Original) The system of claim 12, wherein the dimension is a function of another dimension.

19. (Original) The system of claim 12, further comprising means for using the at least one dimension to evaluate a check rule.

20. (Original) The system of claim 19, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

21. (Currently Amended) A computer program product comprising a computer useable medium having computer readable program code embodied therein, which when executed by a computer system, enables the computer system to model ~~for modeling~~ an integrated circuit, the program product comprising:

program code configured to partition an edge of a shape in the IC design into a plurality of intervals; and

program code configured to assign at least one dimension to each interval;

wherein the partitioning program code includes:

program code configured to generate a core Voronoi diagram for the shape, the core Voronoi diagram being generated based on a L^{∞} metric, the L_{∞} metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points; and

program code configured to partition the edge based on a core element for each vertex of the core Voronoi diagram, the core element being one of a largest possible core element and a smallest possible core element; and.

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

22. (Cancelled).

23-25. (Cancelled).

26. (Currently Amended) The program product of claim ~~22~~ 21, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

27. (Currently Amended) The program product of claim ~~22~~ 21, wherein the at least one dimension is a function of another dimension.

28. (Currently Amended) The program product of claim ~~22~~ 21, further comprising the program code configured to use the dimensions to evaluate a check rule.

29. (Original) The program product of claim 28, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

30. (Currently Amended) An integrated circuit (IC) check rule evaluation system comprising: means for partitioning an edge of a shape in the IC design into a plurality of intervals, the partitioning means including:

means for generating a core Voronoi diagram for the shape based on a L_∞ metric, the L_∞ metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points and

means for partitioning the edge based on a core element for each vertex of the core Voronoi diagram, the core element being one of a largest possible core element and a smallest possible core element;

means for assigning at least one dimension to each interval using a second metric; and

means for using the at least one dimension to evaluate a check rule;

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

31. (Original) The IC check rule evaluation system of claim 30, wherein the check rule is a width dependent spacing rule.